

Charles Moore

Senior Fellow
Advanced Micro Devices, Sunnyvale, CA
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Education:

MSEE, University of Texas at Austin, 1991.
BSEE, Rensselaer Polytechnic Institute, Troy, NY. 1983.

Industry Experience:

Advanced Micro Devices, Sunnyvale, CA, Senior Fellow

02/04 – Present: Chief architect for next generation x86 processor. Management responsibilities for all architecture activities in the California Design Center including Opteron derivative designs, AMD64 architecture, and future architecture extensions.

University of Texas at Austin, Austin, TX, Senior Research Fellow

05/02 – 02/04: Unique two year appointment for research into advanced computer architecture with the goal of transferring technology innovations back into industry.

Chicory Systems, Inc, Austin, TX, Vice President of Engineering

03/01 - 05/02: Responsible for IP delivery of the *MachStream Java Accelerator*, and for the development of new IP for the mobile computing space. After acquisition by Parthus Technologies (Dublin, Ireland) in May 2001, became Vice President of Engineering for the Application Processing Division in the combined company. Management responsibility for 80 person engineering team in Austin, San Jose and Dublin.

IBM Corporation, Austin, TX, Distinguished Engineer

04/00 - 03/01: Next Generation Microprocessor Development. Responsible for concept development on next generation microprocessor, POWER6, optimized for Server applications.

01/98 - 04/00: Chief engineer on IBM's POWER4 project. Responsible for leading chip global leadership team and addressing all critical development issues.

09/96 - 01/98: Lead POWER4 Chip Architect. Responsible for PowerPC-AS Architecture refinements, coordination of performance modeling efforts, and co-lead for the overall microarchitecture.

11/94 - 12/96: Chief Engineer for the PowerPC 641 "Habanero" project. Responsible for technical coordination and development. Project did not complete but brought forward large numbers of patents to the IBM patent portfolio.

01/94 - 10/94: Assessment Lead for the PowerPC "Bellatrix" Processor Development. Responsible for thorough assessment of troubled project, and offering recommendations to management for recovery. Participated in decision process that led to the termination of the project.

07/91 - 12/93: Chief Engineer and project co-lead for the PowerPC 601 Microprocessor. Responsible for leading team to design, verify and implement the first PowerPC chip on an accelerated 10 month

development schedule. This processor was heavily used in the first Apple Power Macintosh machines, the IBM RS/6000 Model 250 workstation, and the first RS/6000 SMP servers.

11/89 - 03/91: Lead implementation engineer for the RSC microprocessor. Responsible for coordinating the technical recovery of IBM's first single-chip version of the POWER architecture. This chip was later mapped into a radiation-hardened technology and used as the central processor for the highly successful Mars Pathfinder mission.

07/86 - 11/89: Power-1 and Power-2 processor development design team member. Participated in the development of the ICU chip and the overall design methodology. Initially acted as member of design team and worked up to lead designer for subsequent technology remaps.

Honors and Awards:

09/02 IBM Faculty Partnership Award
05/02 Appointed *Senior Research Fellow* at UT-Austin
01/01 Named as *IBM Master Inventor*
04/00 Promotion to *IBM Distinguished Engineer*
10/95 Elected to the *IBM Academy of Technology*

Significant Talks:

- 2003 IEEE Vail Computer Elements Workshop. Invited talk – “TRIPS Overview”
- 2003 Workshop on Complexity Effective Design (WCED), Keynote speech – “Managing the Transition from Complexity to Elegance”
- 2003 IEEE ISSCC. Invited talk – “Wire Delay Scalable Microprocessor Architecture for High Performance Systems” in the Technology Directions Session.
- Hot Chips 2001, Program Committee Member and Session Chair for Microprocessor session.
- Microprocessor Forum 2000. “POWER4 Core and Cache Microarchitecture”. Voted by conference participants as one of the top five presentations at the conference.
- Hot Chips 2000, Program Committee Member and Session Chair for Microprocessor session.
- Microprocessor Forum 1999. Invited panelist for "Server System Architecture Trends" panel.
- IEEE Vail Computer Elements Workshop 1999. Invited paper on "Server Oriented Microprocessor Optimizations".
- Microprocessor Forum 1998. Invited panelist for "Future Computer Architecture Trends". Provided first public description of IBM's Gigaprocessor (POWER4) project.
- Microprocessor Forum 1992. First public disclosure of the PowerPC 601 microprocessor.

Publications:

- 09/04 IEEE Micro Magazine, Invited short paper on “Managing the Transition from Complexity to Elegance”
- 06/03 IEEE ISCA Conference. Co-authored paper on “Exploiting ILP, DLP and TLP in the TRIPS Architecture”
- 02/03 IEEE ISSCC Conference. Co-authored paper on “A Wire Delay Scalable Microprocessor Architecture for High Performance Systems”
- 07/94 IBM Journal of Research and Development. Co-authored paper on "Design Aspects of the PowerPC 601 Microprocessor"
- 05/94 Communications of the ACM. Co-authored paper on "The PowerPC Alliance".
- 08/93 IEEE Micro Magazine. Co-authored paper on "Machine Organization of the PowerPC Microprocessor"
- 02/93 IEEE Compcon 1993. Authored and presented paper on "The PowerPC 601 Microprocessor"
- 10/92 IEEE ICCD 1992. Co-authored paper on "The RISC Single Chip (RSC) Microprocessor"
- 10/89 IEEE ICCD 1989. Co-authored paper on "IBM Second Generation RISC Processor (RIOS-1)"

Patents:

Granted 12 US patents (details available upon request)
24 Additional US patents pending

Industry Organizations:

IEEE, Senior Member
ACM, Member
IEEE Micro Magazine Editorial Board

References Available Upon Request